ρ-VEX: A parameterizable and reconfigurable VLIW processor core for Molen

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1 Assignment

1.1 Introduction

For my MSc project at the Computer Engineering Laboratory at Delft University of Technology I will design and implement a reconfigurable Very Large Instruction Word (VLIW) processing core, for use within the Molen[6, 9] reconfigurable processing paradigm. The Instruction Set Architecture (ISA) used for this processing core will be VEX[2] (VLIW Example), which is loosely modeled on the ISA of the HP/ST Lx[1] family of VLIW embedded cores.

1.2 Background

1.2.1 The VEX ISA

The VEX ISA offers a scalable technology platform for embedded VLIW processors, that allows variation in many aspects, including instruction issue width, organization of functional units, and instruction set. The VEX ISA supports a multi-cluster implementation, where each cluster provides a separate (possibly different) VEX ISA implementation. Each cluster has the ability to issue multiple operations in the same instruction. A VEX multi-cluster processor shares one instruction fetch unit and one memory controller. The customizability of the instruction set enables the definitions of special-purpose instructions in an organized way. Figure 1 shows the structure of a VEX multi-cluster implementation.

A VEX Toolchain[7] is provided by Hewlett-Packard Laboratories, which offers a VEX C compiler and a VEX simulator. The compiler allows the user/designer to adjust parameters of the VEX processor (like the number of clusters) easily. The VEX simulator offers an architecture-level simulator which comes with a set of POSIX-like libraries, a cache simulator and an API.

1.2.2 The Molen reconfigurable processor

The Molen paradigm provides a solution to the growing processor hardware design challenges, by reconfigurable processors (processors that adapt their

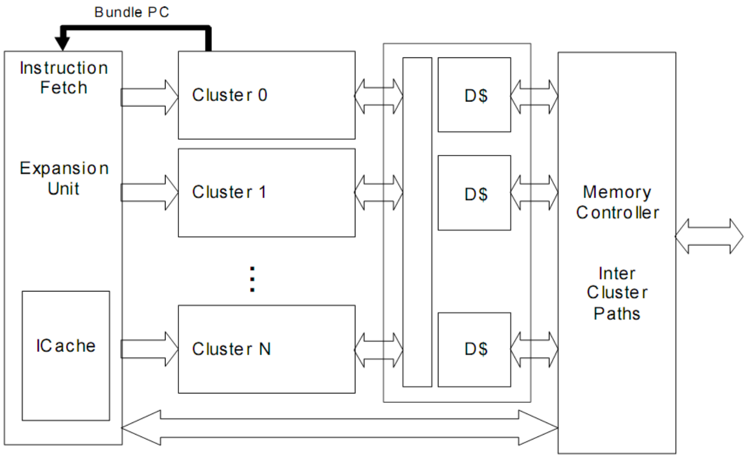

Figure 1: Structure of a VEX multi-cluster implementation [2]

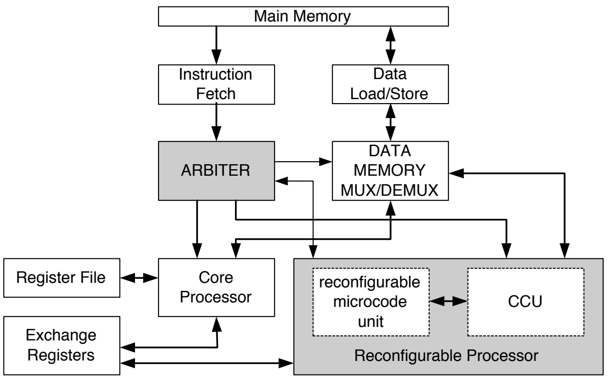

Figure 2: The Molen machine organization[6]

micro-architecture according to the application's requirements). This is being achieved by Custom Configured hardware Units (CCUs) and reconfigurable microcode ($\rho\mu$-code)[8]. Figure 2 presents an overview of the Molen machine organization, including a General Purpose Processor (GPP) with a fixed instruction set, and a reconfigurable co-processor. A prototype[5] of the Molen processor is currently available, based on the Xilinx Virtex-II Pro[10] platform. This FPGA platform features two PowerPC 405[11] general purpose CPU cores are embedded in the reconfigurable fabric (only one is currently used in the prototype).

1.3 Goals

The goal of my research is to explore the design space and the advantages of a parameterizable and reconfigurable VLIW processor (which shall be called ρ-VEX hereafter) within a Molen reconfigurable processing machine. This embedded ρ-VEX processor will not be used for general purpose tasks,

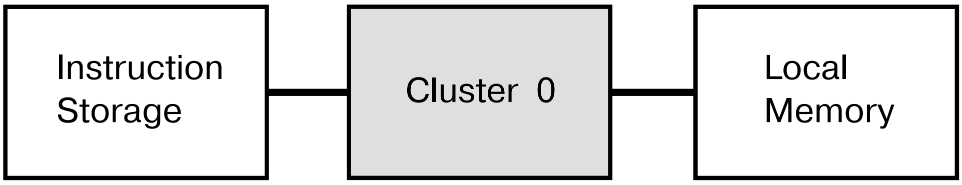

Figure 3: The ρ-VEX single-cluster structure

but for extracted kernels within applications. ρ-VEX will provide a robust and efficient trade-off between flexibility (by means of the existing VEX toolchain) and speed (ASIC (Molen CCU) Vs *VLIW (ρ-VEX)* Vs RISC (GPP in Molen)).

To achieve this I will first investigate what the pay-off is of multiple VEX clusters inside a ρ-VEX processor, keeping in mind its needs, and host platform characteristics. This will be done using the compiler and simulator by HP, and GNU profiling tools. Based on the benchmarks done in [1], the results are likely to be that a 1- or 2-cluster ρ-VEX will result in the best trade-off. Possibilities to parameterize the ρ-VEX are also investigated.

After exploring the pay-off of multiple VEX clusters, a decision will be made about the ρ-VEX design to be implemented as a Molen CCU. An investigation should be made about the completeness of the adopted instruction set, depending on practical criteria such as available design time, on-chip area usage and critical path delay.

After design choices are made, a ρ-VEX prototype will be implemented. This CCU has to be compatible with the current Molen prototype, based on the Xilinx Virtex-II Pro[10] platform. As this prototype does currently not use $\rho\mu$-code to instruct a CCU, a separate instruction storage has to be implemented for the ρ-VEX CPU. Also, a separate small BRAM-based memory will be implemented within ρ-VEX. This memory has not to be very large, because in first instance only small software kernels will be executed by this processor (in the prototype). Depending on the results of the simulator research, a decision will be made about a 1- or 2-cluster implementation. This prototype will not be parameterizable. Figure 3 depicts a ρ-VEX single-cluster structure.

After the implementation of the ρ-VEX CCU, an integration of the VEX toolchain and the Molen toolchain should be thought of.

1.4 Preliminary work

As far as we know, there are no current implementations of a VEX based VLIW processor in an FPGA. Implementations like Spyder[3] and [4], a NIOS II based implementation, do not offer the parameterizable VLIW clusters as the ρ-VEX is aimed to provide.

The idea behind this project originated after a cooperation between Dr.ir. S. Wong (Delft University of Technology) and Prof. G. Brown (Indiana University). Prof. G. Brown was one of the designers of the Lx ISA at the Hewlett-Packard Laboratories.

1.5 Project details

The following persons will be of great importance during the project:

- **Supervisor:** Dr.ir. S. Wong (Delft University of Technology, Computer Engineering Laboratory)
- **Advisor:** Prof. G. Brown (Indiana University, Department of Computer Science)

2 Project Milestones

The following milestones[1] have to be achieved during the project:

- Pay-off exploration of multiple VEX-clusters
- Design choices for ρ-VEX Molen CCU
- Hardware implementation of ρ-VEX Molen CCU
- Integration of ρ-VEX Molen CCU in the Molen prototype

3 Deliverables

At the end of the MSc project, the following deliverables should be presented:

- ρ-VEX processor core implemented as a Molen CCU
- Paper about ρ-VEX FPGA implementation (with instruction storage and small memory)
- Paper about ρ-VEX Molen implementation (inside the current Molen prototype)
- MSc thesis
- Thesis presentation

4 Project Trajectory

During the project, regular meetings will take place with my supervisor Dr.ir. S. Wong. I will keep track of my progress by posting important documents on my homepage at the CE Laboratory website:
`http://ce.et.tudelft.nl/~thijs/`

[1]The milestones are presented in bold in the Expected Timetable (Section 5)

5 Expected Timetable

The timetable will be more fine-tuned after more design constraints are determined.

Date	Milestone
19/11/2007	**Start of project**
	Research about embedded VLIW design and the VEX ISA
	Experimenting with VEX compiler/simulator toolchain
25/01/2008	**Pay-off exploration of multiple VEX-clusters**
22/02/2008	**Design choices for ρ-VEX Molen CCU**
25/04/2008	**Hardware implementation of ρ-VEX Molen CCU**
27/06/2008	**Integration of ρ-VEX Molen CCU in the Molen prototype**
	Writing MSc thesis
18/07/2008	Draft MSc thesis
08/2008	**MSc thesis**
	Preparing presentation
08/2008	**Presentation**

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